# Prototyping Reed Solomon Codes (15,9) on FPGA

By
Th. Prima Ari Setyani *), Bambang Sutopo **)
*) Electrical Engineering, Sanata Dharma University
**) Electrical Engineering, Gadjah Mada University

Extended abstract

Reed Solomon codes are powerfull non binary error correcting codes. This code has wide use in wireless Communications and digital recordings. This research focused on burst errors that most accur in wireless communications cuased by fading effects. The large variations in signal power at the receiver due to channel fading require that the error coding system is able to vary the code parameter in real time. Reed Solomon codes used in digital communication systems have code symbols from Galois field GF($2^m$). Each symbols is made up of m bits. A t error correcting Reed Solomon code has the following parameters : block length :n=2m-1, number of parity symbols :n-k=2t, k represents the number of data symbols, t refers to number of symbols that can be corrected.

In this paper we describe the prototyping of a (15,9) RS codec (*encoder and decoder*) operates over Galois field GF($2^4$). Hence every codeword comprises 9 information symbols, 6 symbols for parity, each symbol is represented by 4 bit. This code can therefore correct up to 3 symbol errors in each codeword. The RS code was initially implemented using a computer. However in order to reduce the size and power requirement of the system and to increase the data rate, we decided to implement the codec in hardware. We choose FPGA because of its ability to reconfigurable, relative low cost and fast designing compare than full custom technology ASIC.

The architectur of RS codec is consisted of encoding section generating RS code, and decoding section generating corrected code. The design of encoding section is relatively straighforward, but the design of the decoders are more complicated. The decoding algorithm comprised four distinct sub-processes : syndrom calculation, calculation of the error locator polynomial, generation of the errror patern, and calculation of these error paterns through inverse transform. These error paterns were than added to the received word to obtain the estimated original information word.

The RS codec were designed using OrCAD Version 9.0 schematics design based on gate circuits for simulation, and implemented on Xilinx FPGA.

To implement the design in Xilinx FPGA we need 865 CLBs or 12460 gates. The available of CLB in Xilinx FPGA XC4013 is only 546, so to implement this design on XC4013 we need two chips. Recapitulation of each process in the encoder and decoder are : Encoder : 30 CLB, Syndrome : 53 CLB, Chien's circuit for error locator : 38 CLB, polynomial for error patern : 26 gate, Berlekamp-Massey algorithm for key solution : 460 CLB, Error paterns invers transform : 250 CLB.

This paper describes how to design RS codec on FPGA and many difficulties we have met in using FPGA. At least this experience encourages us to explore more algorithm that use less hardware, so it can be implemented in one chip FPGA.

References :


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